# HARMONIC ORIENTATION OF PULSE WIDTH MODULATION TECHNIQUE IN MULTILEVEL INVERTERS

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**Abstract.** *The Multilevel Inverter topology gives the advantages of usage in high power and high voltage application with reduced harmonic distortion without a transformer. This paper presents a comparative study of orientation of higher ordered harmonics with increase in switching frequency around the frequency modulation index of nine level diode clamped inverter for different Switching frequency Multicarrier Pulse width Modulation.*

## Keywords

***Multicarrier pulse width modulation, diode clamped inverter, switching frequency optimal PWM, sub-harmonic PWM, constant switching frequency, harmonic orientation, multilevel converter, total harmonic distortion.***

## 1. Introduction

Multilevel Pulse Width Modulation (PWM) inverters have been gained importance in high performance power applications without requiring high ratings on individual devices, as static var compensators, drives and active power filters. A multilevel inverter divides the dc rail directly or indirectly, so that the output of the leg can be more than two discrete levels. As both amplitude modulation and pulse width modulation are used in this, the quality of the output waveform gets improved with low distortion. The advantages of multilevel inverter are good power quality, low switching losses, reduced output dv / dt and high voltage capability. Increasing the number of voltage levels in the inverter increases the power rating. The three main topologies of multilevel inverters are the Diode clamped inverter, Flying capacitor inverter, and the Cascaded H-bridge inverter [1], [2], [3]. The PWM schemes of multilevel inverters are classified in to two types the multicarrier sub-harmonic PWM (MC-SHPWM) and the Multicarrier switching frequency optimal pulse width modulation (MC-SFOPWM) [4], [5]. The MC-SHPWM diode clamped multilevel inverter strategy reduced total harmonic distortion at high switching frequency [6]. This paper considered the most popular structure among the transformer less voltage source multilevel inverters, the diode-clamped converter based on the neutral point converter proposed by Akagea et al [1].

## 2. Multilevel Inverter Illustration

Figure 1(a) shows a two level inverter. Figure 1(b) shows a three level inverter. Figure 1(c) shows N level inverter. All the capacitors comprises to a voltage of $V_{dc}$.

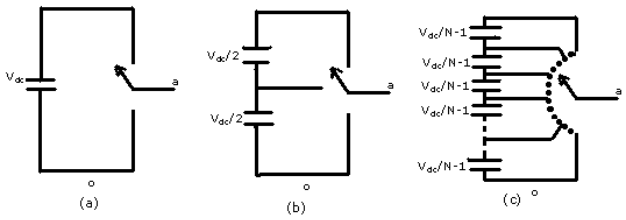


**Fig. 1:** Schematic Diagram of (a) Two level inverter (b) Three level inverter (c) N level inverter.

Figure 2 (a) shows the output voltage of a two level inverter. Figure 2 (b) shows the output voltage a three level inverter. Figure 2 (c) shows the output voltage of an N level inverter.

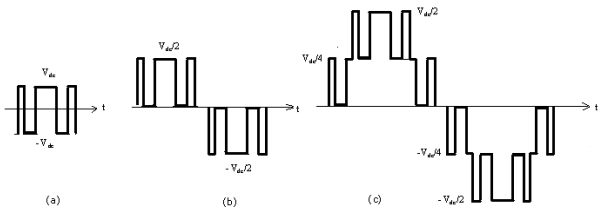


**Fig. 2:** Output voltage of (a) Two level inverter (b) Three level inverter (c) Five level inverter.

### 2.1 Diode Clamped Multilevel Inverter

The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1. \quad (1)$$

The number of levels in the line to load neutral of a star or wye load will be

$$p = 2k - 1. \quad (2)$$

The number of capacitors required, independent of the number of phase, is

$$N_{cap} = N - 1. \quad (3)$$

While the number of clamping diodes per phase is

$$D_{clamp} = 2(N - 1). \quad (4)$$

The number of possible switch states is $n_{states}=N^{phases}$

$$n_{states} = N^{phases}. \quad (5)$$

and the number of switches in each leg is $S_n=2(N-1)$

$$S_n = 2(N - 1). \quad (6)$$

# 3. PWM Methods for Multilevel Inverters

The two basic approaches used to generate the PWM signals for multilevel inverters are

1. Sub Harmonic or Sub-Oscillation carrier based PWM-modulating waveform comparison with offset triangular carriers,
2. Space Vector PWM-space vector modulation based on a rotating vector in multilevel space

and these are the extensions of traditional two level control strategies to several levels.

The main advantages of PWM inverters in comparison to square-wave inverters are (i) control over output voltage magnitude (ii) reduction in magnitudes of unwanted harmonic voltages (iii) improved power factor with unity displacement factor. Lowest order harmonic elimination is possible by proper choice of the number of pulses per half cycle.

Carrara considered different methods of disposing the many carrier bands required in multilevel PWM.

Four alternative carrier PWM strategies with differing phase relationships for a multilevel inverter [15] are as follows:

1. In-phase disposition (IPD), where all the carriers are in phase;
2. Phase opposition disposition (POD), where the carriers above the zero reference are in phase, but shifted by $180^0$ from those carriers below the zero reference;
3. Alternative phase opposition disposition (APOD), where each carrier band is shifted by $180^0$ from the adjacent bands;
4. Phase Disposition (PD), all the carriers are phase shifted by $2\pi/(N-1)$ radians.

PD strategy is used most frequently because it produces minimum harmonic distortion for the line–to–line output voltage [13], [14], [15].

## 3.1 Sub Harmonic Pulse Width Modulation (SHPWM) Technique or Sinusoidal Pulse Width Modulation (SPWM)

In SHPWM technique the intersection of the triangular carrier and the modulation wave determines the generation of the pulse. This requires a carrier of much higher frequency than the modulation frequency. The generated rectilinear output voltage pulses are modulated such that their duration is proportional to the instantaneous value of the sinusoidal waveform at the centre of the pulse; that is, the pulse area is proportional to the corresponding value of the modulating sine wave.

Good quality output voltage in SPWM requires the modulation index (MI) to be less than or equal to 1,0. For MI > 1 (over-modulation), the fundamental voltage magnitude increases but at the cost of decreased quality of output waveform. The maximum fundamental voltage that the SPWM inverter can output (without resorting to over-modulation) is only 78,5 % of the fundamental voltage output by square-wave inverter. In this paper SPWM technique has been considered. The merits and demerits of this PWM technique for different frequencies are compared under comparable circuit conditions on the basis of factors like (i) quality of output voltage (ii) obtainable magnitude of output voltage (iii) ease of control (iv) reduction in total harmonic distortion etc. The peak obtainable output voltage from the given input dc voltage is one important figure of merit for the inverter.

If the carrier frequency is very high, an averaging effect occurs, resulting in a sinusoidal fundamental output with high-frequency harmonics, but minimal low-frequency harmonics.

## 3.2 Switching Frequency Optimal Pulse width Modulation (SFOPWM) Technique

Steinke [12] proposed SFOPWM, a carrier based method where addition of triplen harmonic to the fundamental frequency Sinusoidal lowers the peak magnitude, thus allowing operating in over modulation region. This increases the inverter output voltage without compromising on the quality of the output waveform [3], [4].

Equations (7) to (10) are used to obtain the modulating wave.

$$V_{offset} = \frac{(\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c))}{2}. \quad (7)$$

$$V_{aSFO} = V_a - V_{offset}. \quad (8)$$

$$V_{bSFO} = V_b - V_{offset}. \quad (9)$$

$$V_{cSFO} = V_c - V_{offset}. \quad (10)$$

The zero sequence modification made by the SFOPWM technique restricts its use to three phase three wire system; however it enables the modulation index to be increased by 15,47 % before over modulation or pulse dropping occurs.

The amplitude modulation index and frequency modulation index are given in (11) and (12) respectively.

$$MI \vee m_a = \frac{A_m}{(m-1)A_c}. \quad (11)$$

$$m_f = \frac{f_c}{f_m}. \quad (12)$$

Where:

- $m$ is the number of carrier waves also the level of the inverter, required for pulse generation
- $A_m$ and $f_m$ are the amplitude and frequency of the reference wave, a sinusoidal wave respectively
- $A_c$ and $f_c$ amplitude of the carrier wave, a triangular wave respectively

## 4. Analysis of Nine Level Diode Clamped Inverter

A three-phase nine-level diode-clamped inverter is shown in Fig. 4. Each phase is constituted by 16 switches (eight switches for upper leg and eight switches for lower leg). Switches $S_{a1}$ through $S_{a8}$ of upper leg form complementary pair with the switches $S_{a1}'$ to $S_{a8}'$ lower leg of the same phase.

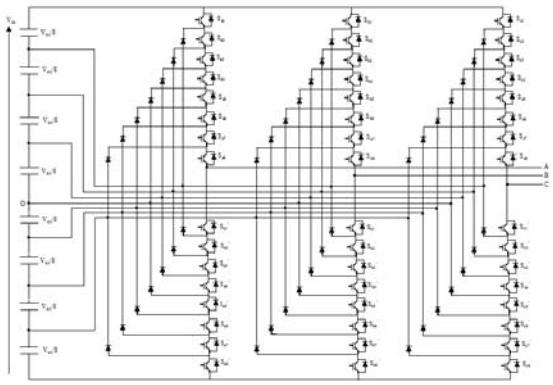

**Fig. 3:** Circuit diagram of 3 phase nine level diode clamped inverter.

The complementary switch pairs for phase 'A' are ($S_{a1}$, $S_{a1}'$), ($S_{a2}$, $S_{a2}'$), ($S_{a3}$, $S_{a3}'$), ($S_{a4}$, $S_{a4}'$), ($S_{a5}$, $S_{a5}'$), ($S_{a6}$, $S_{a6}'$), ($S_{a7}$, $S_{a7}'$), ($S_{a8}$, $S_{a8}'$) and similarly for B and C phases [1], [2], [3], [4], [5], [6], [7], [8], [17]. Clamping diodes are used to carry the full load current.

Table 1 shows phase to fictitious midpoint 'o' of capacitor string voltage ($V_{AO}$) and line to line voltage ($V_{AB}$) for various switching.

**Tab.1:** Pole voltage and line voltage of a nine level inverter.

| $S_{a1}$ | $S_{a2}$ | $S_{a3}$ | $S_{a4}$ | $S_{a5}$ | $S_{a6}$ | $S_{a7}$ | $S_{a8}$ | $V_{AB}$ | $V_{AO}$ |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $V_{dc}$ | $V_{dc}$ |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $V_{dc}/8$ | $3V_{dc}/4$ |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | $2V_{dc}/8$ | $2V_{dc}/4$ |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | $3V_{dc}/8$ | $V_{dc}/4$ |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | $4V_{dc}/8$ | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | $5V_{dc}/8$ | $-V_{dc}/4$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | $6V_{dc}/8$ | $-2V_{dc}/4$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | $7V_{dc}/8$ | $-3V_{dc}/4$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $-V_{dc}$ |

This paper provides analytical methods for the study, performance evaluation, and design of the carrier-based PWM which are widely employed in PWM multilevel voltage-source inverter drives due to the low-harmonic distortion waveform characteristics with well-defined harmonic spectrum, the fixed switching frequency, and implementation simplicity. The one most important modulator characteristics the total harmonic distortion is analytically modeled and compared for various switching frequencies applied to a Nine Level Neutral Point Clamped or Diode Clamped Inverter. Simulations of the controller and of the inverter have been made in the MATLAB SIMULINK environment.

A Nine Level Neutral Point Clamped or Diode Clamped Inverter is simulated for different switching frequencies and the orientation of higher ordered harmonics around the switching frequency is presented.

## 5. Simulation Results and Discussions

A Nine Level Diode Clamped Inverter is simulated for a modulation index of 0,9 and switching frequencies of 1 kHz, 2 kHz, 3 kHz and 4 kHz and the orientation of higher ordered harmonics around the switching frequency is presented.

For $f_c = 1$ kHz, the Total Harmonic Distortion is 14,32 %. Figure 4 indicates 20$^{th}$ harmonic is the dominant and constituting maximum value of the THD and is 10,57 % shown in Tab. 2.

When $f_c = 2$ kHz, the Total Harmonic Distortion is 14,09 %. Figure 6 indicates 30$^{th}$ harmonic is the significant and constituting maximum value of the THD and it is 10,41 % shown in Tab. 3.

Figure 8 shows when $f_c$ increases to 3 kHz, the Total Harmonic Distortion is 13,90 % where 40th harmonic is the dominant and constituting maximum value of the THD and is 10,12 % shown in Tab. 4.

From Tab. 5 the significant 80th harmonic value is 9,99 % of Total Harmonic Distortion 13,77 % and is shown in Fig. 7 for $f_c = 4$ kHz.

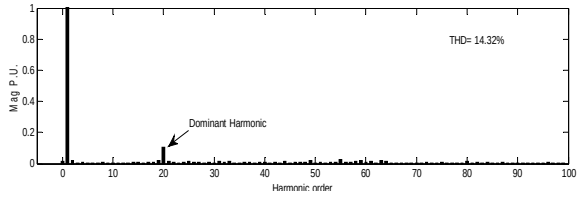


**Fig. 4:** Pole voltage THD $m_f$ = 20, $fc$ = 1 kHz.

**Tab.2:** List of harmonic orientation around $f_C$ = 1 kHz.

| | | |
|---|---|---|
| 700 Hz (h14): | 0.95% | 81.8° |
| 750 Hz (h15): | 0.73% | 122.5° |
| 800 Hz (h16): | 0.53% | 0.0° |
| 850 Hz (h17): | 1.04% | 161.0° |
| 900 Hz (h18): | 1.02% | 84.9° |
| 950 Hz (h19): | 1.76% | 182.0° |
| 1000 Hz (h20): | 10.57% | 267.7° |
| 1050 Hz (h21): | 1.44% | 183.2° |
| 1100 Hz (h22): | 0.90% | 91.3° |
| 1150 Hz (h23): | 0.29% | 0.0° |
| 1200 Hz (h24): | 0.94% | 0.0° |
| 1250 Hz (h25): | 1.26% | 0.0° |
| 1300 Hz (h26): | 0.99% | 90.4° |

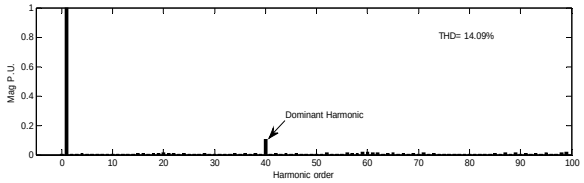


**Fig. 5:** Pole voltage THD $m_f$ = 40, $fc$ = 2 kHz.

**Tab.3:** List of harmonic orientation around $f_c$ = 2 kHz.

| | | |
|---|---|---|
| 1700 Hz (h34): | 0.78% | 88.3° |
| 1750 Hz (h35): | 0.19% | 57.1° |
| 1800 Hz (h36): | 0.83% | 0.0° |
| 1850 Hz (h37): | 0.14% | 59.1° |
| 1900 Hz (h38): | 0.81% | 96.3° |
| 1950 Hz (h39): | 0.04% | 65.5° |
| 2000 Hz (h40): | 10.41% | 267.7° |
| 2050 Hz (h41): | 0.01% | 78.8° |
| 2100 Hz (h42): | 0.87% | 97.6° |
| 2150 Hz (h43): | 0.03% | 173.4° |
| 2200 Hz (h44): | 0.88% | 0.0° |
| 2250 Hz (h45): | 0.01% | 119.7° |
| 2300 Hz (h46): | 0.83% | 91.0° |
| 2350 Hz (h47): | 0.02% | 18.2° |

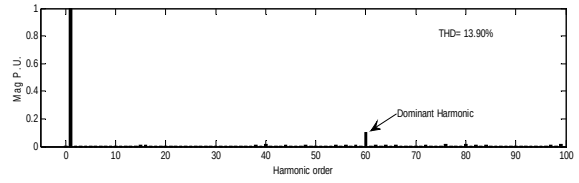


**Fig. 6:** Pole voltage THD $m_f$ = 60, $fc$ = 3 kHz.

**Tab.4:** List of harmonic orientation around $f_C$ = 3 kHz.

| | | |
|---|---|---|
| 2700 Hz (h54): | 0.75% | 95.9° |
| 2750 Hz (h55): | 0.08% | 0.0° |
| 2800 Hz (h56): | 0.92% | 0.0° |
| 2850 Hz (h57): | 0.08% | 0.0° |
| 2900 Hz (h58): | 0.91% | 95.8° |
| 2950 Hz (h59): | 0.08% | 0.0° |
| 3000 Hz (h60): | 10.12% | 268.4° |
| 3050 Hz (h61): | 0.05% | 0.0° |
| 3100 Hz (h62): | 0.96% | 94.8° |
| 3150 Hz (h63): | 0.05% | 218.4° |
| 3200 Hz (h64): | 0.94% | 0.0° |
| 3250 Hz (h65): | 0.07% | 203.8° |
| 3300 Hz (h66): | 0.80% | 86.4° |

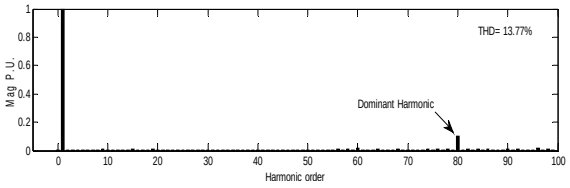


**Fig. 7:** Pole voltage THD $m_f$ = 80, $fc$ = 4 kHz.

**Tab.5:** List of harmonic orientation around $f_C$ = 4 kHz.

| | | |
|---|---|---|
| 3750 Hz (h75): | 0.03% | 150.3° |
| 3800 Hz (h76): | 0.99% | 0.0° |
| 3850 Hz (h77): | 0.06% | 61.7° |
| 3900 Hz (h78): | 0.88% | 91.0° |
| 3950 Hz (h79): | 0.06% | 0.0° |
| 4000 Hz (h80): | 9.99% | 268.7° |
| 4050 Hz (h81): | 0.02% | 210.5° |
| 4100 Hz (h82): | 0.92% | 98.0° |
| 4150 Hz (h83): | 0.06% | 65.9° |
| 4200 Hz (h84): | 1.03% | 0.0° |
| 4250 Hz (h85): | 0.04% | 13.8° |
| 4300 Hz (h86): | 0.89% | 89.8° |

When a triangular carrier wave has its peak coincides with zero of the reference sinusoid there are $P$ number of pulses per half cycle.

$$P = \frac{m_f}{2}. \tag{13}$$

If zero of the triangular carrier wave coincides with zero of the reference sinusoid there is (P - 1) number of pulses per half cycle.

The PWM pushes the harmonics into a high frequency range around the switching frequency $f_c$ and its multiples around $m_f$, $2m_f$, $3m_f$ and so on. The frequencies at which the voltage harmonics occur can be related by

$$f_n = \left(j \cdot m_f \pm K\right) \cdot f_c. \tag{14}$$

Where the nth harmonic equals the kth sideband of jth times the frequency modulation ratio $m_f$.

$$n = j \cdot m_f \pm K = 2jP \pm K, \tag{15}$$

for $j$=1, 2, 3, ... and $k$=1, 2, 3, ...

Harmonic analysis of the output modulated voltage wave reveals that SPWM has the following important features.

For MI < 1, largest amplitudes in the output voltage are associated with harmonics of order $m_f$, $m_f \pm 1$ or

2P ± 1. Thus by increasing the number of pulses per half cycle, the order of dominant harmonic frequency can be raised, which can then be filtered out easily.

For MI > 1, lower order harmonic appear, since the pulse width is no longer a sinusoidal function of the angular position of the pulse. Over modulation basically leads to a square wave operation and adds more harmonics as compared to operation in the linear range (MI ≤ 1).

Figure 8, Fig. 9 and Fig. 10 are the pole, phase and line voltages respectively for 10 pulses per half cycle ($m_f$ = 20).

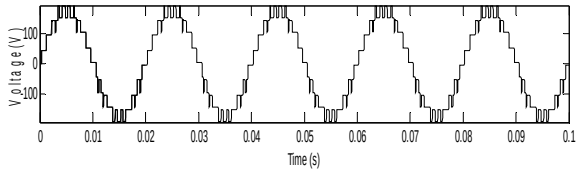


**Fig. 8:** Pole voltage $f_c$ = 1 kHz.

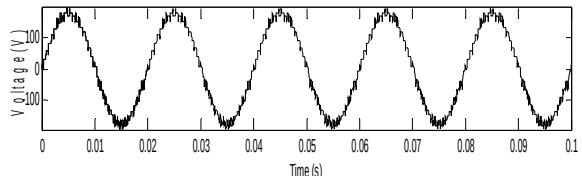


**Fig. 9:** Pole voltage $f_c$ = 2 kHz.

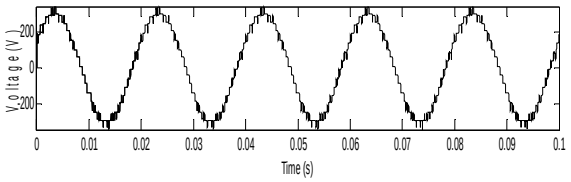


**Fig. 10:** Line voltage $f_c$ =1 kHz.

Figure 11, Fig. 12 and Fig. 13 are the pole, phase and line voltages respectively for 20 pulses per half cycle.

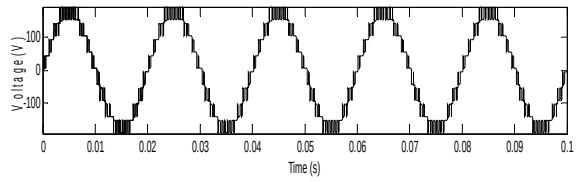


**Fig. 11:** Pole voltage $f_c$ = 2 kHz.

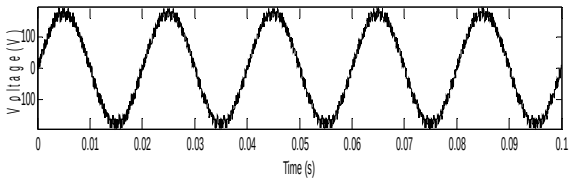


**Fig. 12:** Phase voltage $f_c$ = 2 kHz.

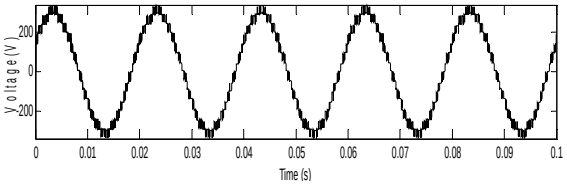


**Fig. 13:** Line voltage $f_c$ = 2 kHz.

Figure 14, Fig. 15 and Fig. 16 are the pole, phase and line voltages respectively for 30 pulses per half cycle.

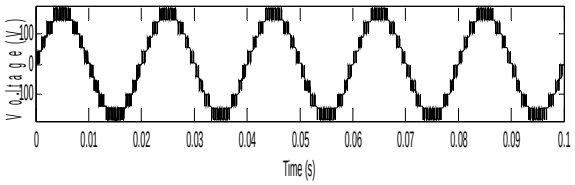


**Fig. 14:** Pole voltage $f_c$ = 3 kHz.

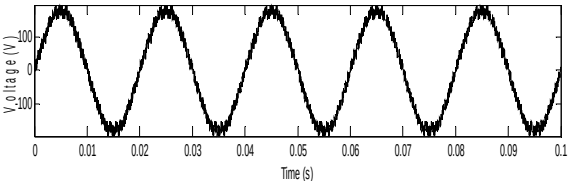


**Fig. 15:** Phase voltage $f_c$ = 3 kHz.

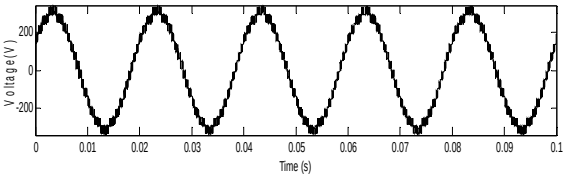


**Fig. 16:** Line voltage $f_c$ = 3 kHz.

Figure 17, Fig. 18 and Fig. 19 are the pole, phase and line voltages respectively for 40 pulses per half cycle.

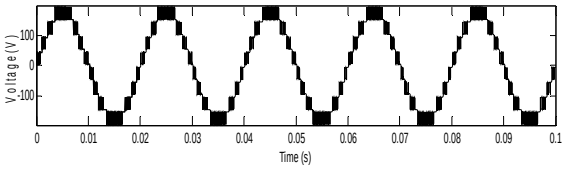


**Fig. 17:** Pole voltage $f_c$ = 4 kHz.

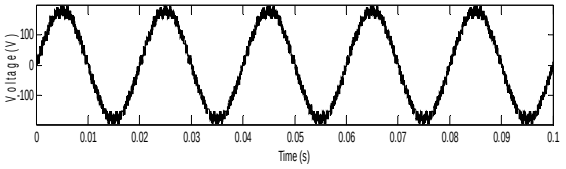


**Fig. 18:** Phase voltage $f_c$ = 4 kHz.

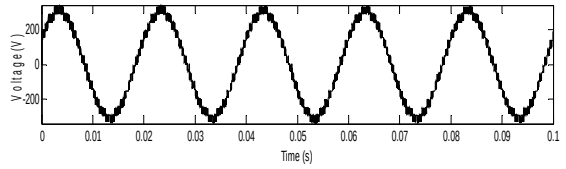


**Fig. 19:** Line voltage $f_c$ = 4 kHz.

## 6. Conclusions

A nine level diode clamped inverter is modeled and simulated for different switching frequencies of SPWM technique and are compared for normal modulation index.

High switching frequency decreases the low ordered harmonics thus increasing the higher ordered harmonics which can be filtered out easily by filters in output voltage.

Increase in switching frequency improves the quality of the output voltage waveform.

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